Amendments To The Claims:

Please amend the claims as follows:

1. (Currently amended) A method including:

in a queue, writing a first ~~instruction~~microinstruction of a plurality of ~~instruction~~microinstructions to a first location indicated by a write pointer, the plurality of ~~instruction~~microinstructions being written to the queue as a set of a predetermined number of ~~instruction~~microinstructions, and the first ~~instruction~~microinstruction of the plurality of ~~instruction~~microinstructions being indicated as invalid on account of being outside a trace of ~~instruction~~microinstructions, the trace of microinstructions corresponding to a macroinstruction and comprising a sequence of microinstructions;

making a qualitative determination whether or not to retain the first ~~instruction~~microinstruction within the queue based on the indicated invalidity of the first ~~instruction~~microinstruction;

if the qualitative determination is to retain the first ~~instruction~~microinstructions, then advancing the write pointer to indicate a second location within the queue into which to write a second ~~instruction~~microinstruction; and

if the qualitative determination is not to retain the first ~~instruction~~microinstruction, then maintaining the write pointer to indicate the first location within the queue into which to write the second ~~instruction~~microinstruction, so that the first ~~instruction~~microinstruction is overwritten by the second ~~instruction~~microinstruction.

2. (Currently Amended) The method of claim 1 wherein the qualitative determination includes examining a valid bit associated with the first ~~instruction~~microinstruction to determine validity of the first ~~instruction~~microinstruction, making the qualitative determination to retain the

first ~~instruction~~microinstruction if the valid bit indicates the first ~~instruction~~microinstruction is being valid, and making the qualitative determination not to retain the first ~~instruction~~microinstruction if the valid bit indicates the first ~~instruction~~microinstruction as being invalid.

3. (Canceled)

4. (Currently Amended) The method of claim 2 wherein a plurality of ~~instruction~~microinstructions are written to the queue in a set of a predetermined number of ~~instruction~~microinstructions, and wherein at least one ~~instruction~~microinstruction of the set is indicated as being invalid on account of a branch misprediction relating to a branch ~~instruction~~microinstruction upstream of the at least one ~~instruction~~microinstruction in a stream of ~~instruction~~microinstructions.

5. (Canceled) ~~The method of claim 1 wherein the first instruction comprises a first microinstruction.~~

6. (Currently Amended) The method of claim ~~5~~ 1 wherein the first microinstruction is written to the queue from a microinstruction cache.

7. (Currently Amended) The method of claim 6 wherein the first microinstruction is part of a trace of microinstructions received from the microinstruction cache.

8. (Currently Amended) The method of claim 6 wherein the first ~~instruction~~microinstruction is received from an ~~instruction~~microinstruction source operating in a first clocking domain into the queue and read from the queue to an ~~instruction~~microinstruction destination operating in a second

clocking domain.

9. (Currently Amended) The method of claim 1 wherein the first ~~instruction~~microinstruction is received into the queue as part of a set of ~~instruction~~microinstructions comprising a first predetermined number of ~~instruction~~microinstructions and read from the queue to an ~~instruction~~microinstruction destination as part of a second set of ~~instruction~~microinstructions comprising a second number of ~~instruction~~microinstructions.

10. (Currently Amended) The method of claim 1 wherein the first ~~instruction~~microinstruction is written from a source to a destination, and wherein the queue comprises a first path between source and destination, the method including propagating the first ~~instruction~~microinstruction from the source to the destination via a second path, not including the queue, if the queue is empty.

11. (Currently Amended) The method of claim 10 including selecting between the first and second paths to receive the first ~~instruction~~microinstruction for propagation to the destination.

12. (Currently Amended) The method of claim 1 wherein the queue includes a first portion to support a first thread within a multithreaded environment and a second portion to support a second thread within the multithreaded environment, and wherein the first location into which the first ~~instruction~~microinstruction is written is located in the first portion if the first ~~instruction~~microinstruction comprises part of the first thread.

13. (Currently amended) Apparatus comprising:

a queue to buffer a first ~~instruction~~microinstruction propagated from a source to a destination; and

B1

write logic to make a qualitative determination whether or not to retain the first ~~instruction~~microinstruction within the queue; if the qualitative determination is to retain the first ~~instruction~~microinstruction, to advance a write pointer to indicate a second location within the queue into which to write a second ~~instruction~~microinstruction; and, if the qualitative determination is not to retain the first ~~instruction~~microinstruction, to maintain the write pointer to indicate the first location within the queue into which to write the second ~~instruction~~microinstruction, so that the first ~~instruction~~microinstruction is overwritten by the second ~~instruction~~microinstruction.;

wherein the first ~~instruction~~microinstruction is written to the queue as part of a set including a predetermined number of ~~instruction~~microinstructions, and wherein at least one ~~instruction~~microinstruction of the set is indicated as being invalid on account of being outside a trace of ~~instruction~~microinstructions, the trace of microinstructions corresponding to a macroinstruction and comprising a sequence of microinstructions.

14. (Currently Amended) The apparatus of claim 13 wherein the write logic is to examine a valid bit associated with the first ~~instruction~~microinstruction to determine validity of the first ~~instruction~~microinstruction, to make the qualitative determination to retain the first ~~instruction~~microinstruction if the valid bit indicates the first ~~instruction~~microinstruction as being valid, and to make the qualitative determination not to retain the first ~~instruction~~microinstruction if the valid bit indicates the first bit as being invalid.

15. (Canceled)

16. (Currently Amended) The apparatus of claim 14 wherein the first

B1

~~instruction~~microinstruction is written to the queue as part of a set of a predetermined number of ~~instruction~~microinstructions, and wherein at least one ~~instruction~~microinstruction of the set is indicated as being invalid on account of a branch misprediction relating to a branch ~~instruction~~microinstruction upstream of the at least one ~~instruction~~microinstruction in a stream of ~~instruction~~microinstructions.

17. (Canceled) ~~The apparatus of claim 1 wherein the first instruction is a first microinstruction.~~

18. (Currently Amended) The apparatus of claim ~~17~~ 1 wherein the source from which the first microinstruction is written to the queue comprises a microinstruction cache.

19. (Canceled) ~~The apparatus of claim 18 wherein the first microinstruction is part of a trace of microinstructions received from the microinstruction cache.~~

20. (Currently Amended) The apparatus of claim 13 wherein the queue comprises a first path between the source and the destination, the apparatus including a second path between the source and destination, not including the queue, and wherein the write logic directs the first microinstruction to be propagated between the source and destination via the second path if the queue is empty.

21. (Currently amended) A machine-readable medium storing a sequence of ~~instruction~~microinstructions that, when executed by machine, cause the machine to perform the steps of:

in a queue, writing a first ~~instruction~~microinstruction of a plurality of ~~instruction~~microinstructions to a first location indicated by a write pointer, the

plurality of ~~instruction~~microinstructions being written to the queue as a set of a predetermined number of ~~instruction~~microinstructions, and the first ~~instruction~~microinstruction of the plurality of ~~instruction~~microinstructions being indicated as invalid on account of being outside a trace of ~~instruction~~microinstructions, the trace of microinstructions corresponding to a macroinstruction and comprising a sequence of microinstructions;

making a qualitative determination whether or not to retain the first ~~instruction~~microinstruction within the queue based on the indicated invalidity of the first ~~instruction~~microinstruction;

if the qualitative determination is to retain the first ~~instruction~~microinstructions, then advancing the write pointer to indicate a second location within the queue into which to write a second ~~instruction~~microinstruction; and

if the qualitative determination is not to retain the first ~~instruction~~microinstruction, then maintaining the write pointer to indicate the first location within the queue into which to write the second ~~instruction~~microinstruction, so that the first ~~instruction~~microinstruction is overwritten by the second ~~instruction~~microinstruction.

22. (Currently Amended) The machine-readable medium of claim 21 wherein the sequence of ~~instruction~~microinstructions cause a multiprocessor to perform the step of examining a valid bit associated with the ~~instruction~~microinstruction to determine validity of the first ~~instruction~~microinstruction, to make the qualitative determination to retain the first ~~instruction~~microinstruction if the valid bit indicates the first ~~instruction~~microinstruction as being valid, and to make the qualitative determination not to retain the first ~~instruction~~microinstruction if the valid bit indicates the first ~~instruction~~microinstruction as being invalid.